DESIGN TECHNIQUE FOR HIGH POWER, HIGH EFFICIENCY, BROADBAND DISTRIBUTED AMPLIFIERS

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J. Bradford Cole
Aryeh Platzker

Raytheon Company
Research Division
131 Spring Street
Lexington, MA 02173
(617) 860-3300

ABSTRACT

Distributed amplifiers, while having uniform gain over a broad frequency range, typically have nonuniform power performance. The Computer Aided Design technique described here was applied to an MMIC distributed power amplifier design with the result that improved efficiency (10-13%) and constant output power (> 25 dBm) was achieved over the 6-18 GHz band, while the conventionally designed circuits show 4-6 dB power degradation.

INTRODUCTION

Since their revival in popularity [1] due to the MMIC revolution, distributed amplifiers have been targeted for a wide range of applications. Their ease of design, good input and output return losses, flat gain over large bandwidths, and relative insensitivity to processing variations have been given as reasons for their popularity [2].

The large signal performance of distributed ampplifiers has not been as favorable, but this is a consequence of using inappropriate optimization goals in the design.

In this paper we present an alternate design methodology, examples of performance improvements expected from using the new design technique, and application of this technique to an MMIC amplifier. We also discuss performance tradeoffs associated with designing distributed power amplifiers.

CONVENTIONAL DESIGN APPROACH TO POWER AMPLIFIER CIRCUITS

The technique often reported [3,4] for designing power distributed amplifiers is to optimize the circuit for small signal gain and input and output return losses, using the largest possible gate periphery that will simultaneously provide the requisite output power with the desired gain at the highest frequency of operation. Regardless of the scheme used to increase the gate periphery, the power performance of conventional circuits is not optimal. Typically power output and efficiency will decrease with increasing frequency.

Figure 1 shows the small signal gain, and input and output return losses of a distributed amplifier stage consisting of six identical cells, each with a 200 μm FET, that has been designed using conventional methods.

Figure 2 shows the calculated output power of this circuit at approximately 2 dB gain compression. The cause of the power degradation becomes apparent if the load impedance seen by each device is calculated versus frequency. Figure 3 is a composite plot of the shunt resistance loading the FETs, and Figure 4 is a composite plot of the shunt capacitances loading each FET. The impedances deviate significantly from the optimum power load which is a parallel RC circuit with R~ 130 Ω and C~ -0.08 pF. The result is generally a rapidly increasing RF drain current with increasing frequency [5,6].

POWER DISTRIBUTED AMPLIFIER DESIGN TECHNIQUE

The optimum load resistance for maximum output power in class-A operation of an idealized FET is

$$R \sim (Vbr + Vp - Vknee)/Imax$$

where Vbr is the gate-drain breakdown voltage, Vp is the pinchoff voltage, Imax is the maximum open channel drain current, and Vknee is the drain voltage at which Imax is reached. The reactive component of the optimum power load is a shunt capacitor, C~ -Cds. These are only approximations, though, because of the non-ideal nature of GaAs FETs.

Using a circuit designed for small signal gain and low return loss as a starting point, the relative individual FET drain voltages and currents versus frequency should first be examined. While the goal of the design is to provide the proper impedance to each device, presently available microwave CAD software restricts consideration to voltages and currents for its analysis and optimization. Nevertheless, a decreasing voltage with constant current versus frequency, or an increasing current with constant voltage versus frequency implies a decreasing impedance, and vice versa, so the end goal is attained indirectly.

In addition to simultaneously optimizing voltages and currents, the amplifier gain must remain flat and at an acceptably high level. Also, since all of the devices should be driven equally hard to optimize power output and overall efficiency, their drain currents should be approximately equal to each other.

In order to achieve the proper power match, it was found that the conventional design approach, where the amplifier stage is composed of identical cells, had to be modified. In general, gate and drain line lengths and impedances, as well as FET peripheries, have to be varied. The drain line termination impedance can also play a significant role.

POWER DISTRIBUTED AMPLIFIER DESIGN EXAMPLE

The technique described was used to modify the 1.2 mm distributed amplifier described above and improve its power performance. Figure 5 shows the shunt resistive components of the device load impedances, and Figure 6 is a composite of the shunt capacitances which load the devices. In this design, the RF drain currents of the FETs remain

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nearly constant with frequency and of equal magnitude, and the RF voltage builds as the signal propagates towards the load. Consequently, the load impedance is naturally lower on the device furthest from the load than on the device closest to the load.

Figure 7 shows the expected small signal gain and the magnitude of the input and output return losses of the design. There has been no significant sacrifice in bandwidth, gain flatness, or input return loss as a result of optimizing the distributed amplifier for power performance. The output return loss degraded, however. This is not surprising since the FETs had to be mismatched for small signal gain to be matched for output power; an analogous situation to that of single-ended amplifiers.

Figure 8 compares the predicted performance of the distributed amplifier circuit examples when the conventional and the improved methods are used. A 6 dB improvement in output power is expected at 18 GHz when the circuit is designed using the technique just described here.

EXPERIMENTAL RESULTS

A two-stage power distributed amplifier, shown in Figure 9, was developed using the power optimization design technique. A first stage consisting of six 120 μm FETs was added to the six 200 μm FET topology described above. The circuits were processed on 4-mil, ion-implanted, GaAs with a doping of $2x10^{17}/cm^3$. The FETs were etched to have a pinchoff voltage of -4 V. The capacitors use 3000A of plasma CVD Si_3N_4, and the thin film resistors are made of evaporated Ti/Pt. All dc blocking and bias bypassing circuitry is on-chip.

Figure 10 shows a measured input return loss of less than -15 dB, and an output return loss which approaches -7 dB. Figure 11 shows the small signal gain and large signal performance. The results are 9 dB ±0.5 dB of gain, 25.0-26.5 dBm (330-450 mW) of output power, and 10-13% power-added efficiency at 2 dB gain compression over the 6-18 GHz band. The power performance is much flatter than that commonly observed in distributed amplifiers and agrees well with design predictions.

CONCLUSION

It has been shown that the power performance of distributed amplifiers can be greatly improved by designing the circuit such that the proper power match is presented to each device across the entire frequency range. This condition is usually not fulfilled when the amplifier is designed for optimal small signal characteristics. Small signal techniques have been used, however, to provide the proper power performance load impedance to each device.

ACKNOWLEDGEMENTS

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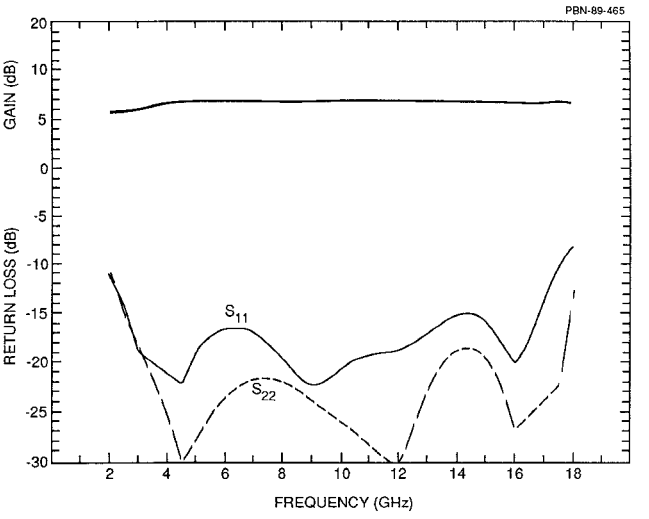

Figure 1. Gain and Return Loss of Distributed Amplifier Stage Designed for Small Signal Performance.

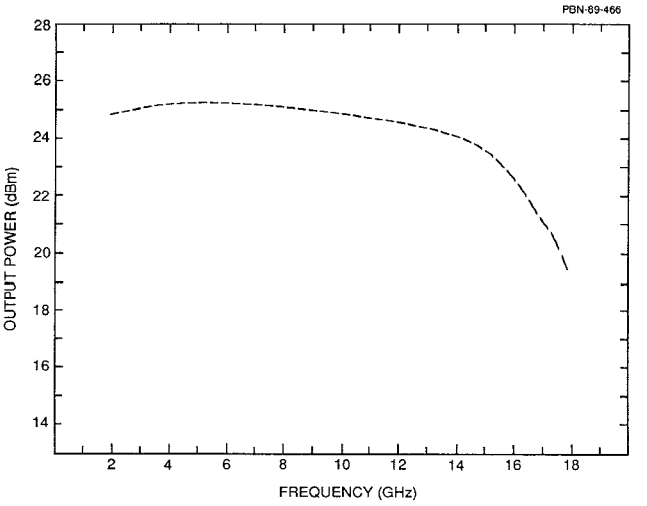

Figure 2. Predicted Power Performance of Distributed Amplifier Designed for Small Signal Performance.

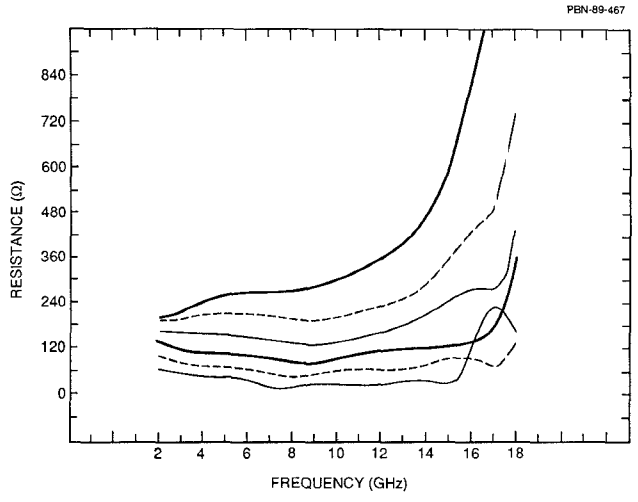

Figure 3. Shunt Resistive Component of FET Load Impedances in Distributed Amplifier Designed for Small Signal Performance.

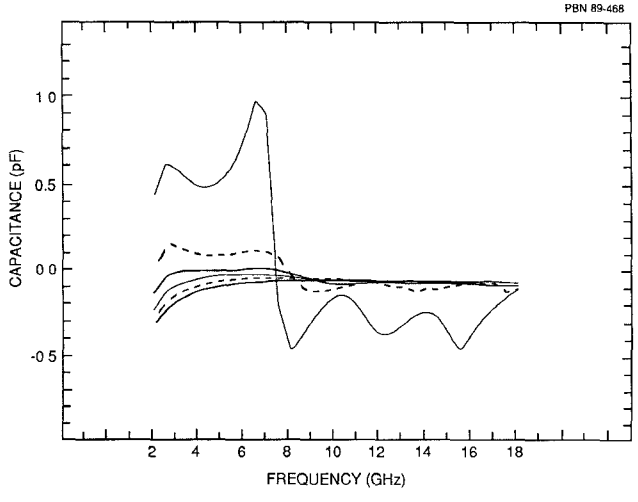

Figure 4. Shunt Capacitance of FET Load Impedances in Distributed Amplifier Designed for Small Signal Performance.

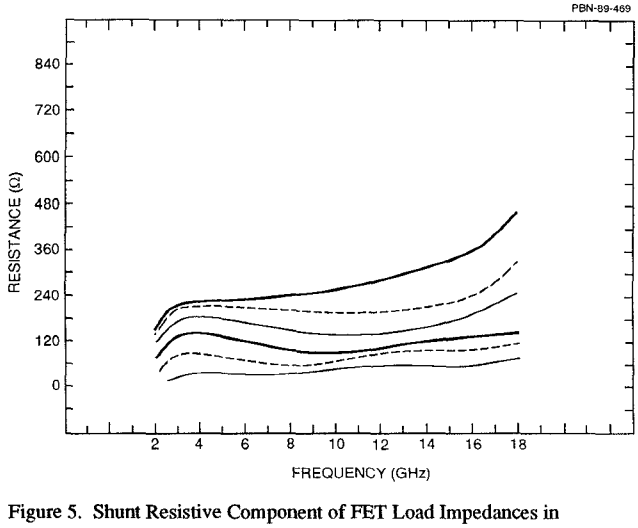

Figure 5. Shunt Resistive Component of FET Load Impedances in Distributed Amplifier Designed for Small Signal Performance.

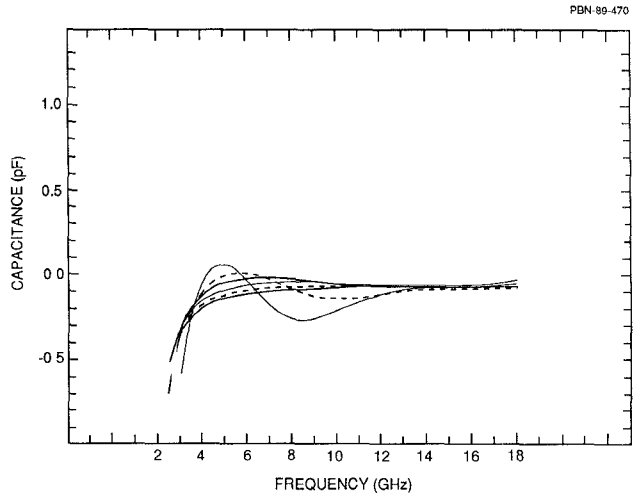

Figure 6. Shunt Capacitance of FET Load Impedances in Distributed Amplifier Designed for Small Signal Performance.

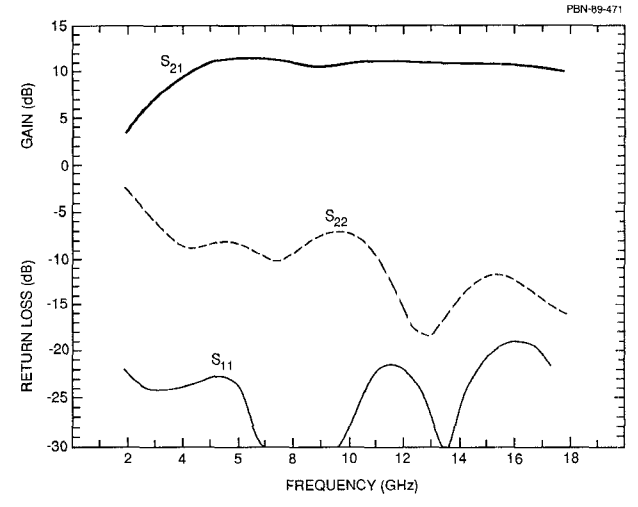

Figure 7. Gain and Return Loss of 2-Stage Distributed Amplifier Circuit Designed for Power Performance.

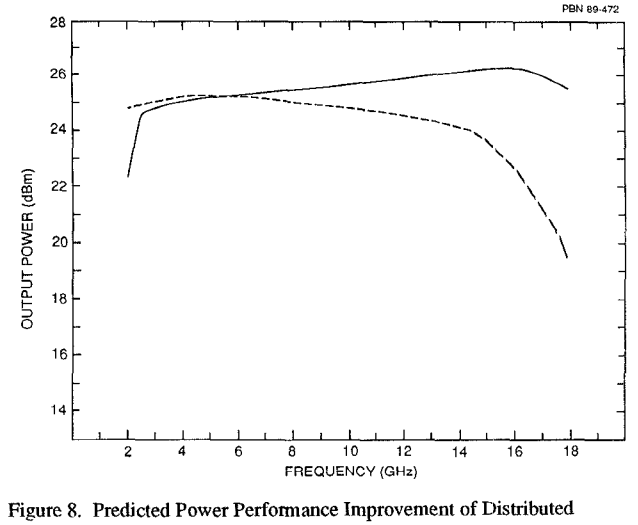

Figure 8. Predicted Power Performance Improvement of Distributed Amplifiers Designed for Power Performance.

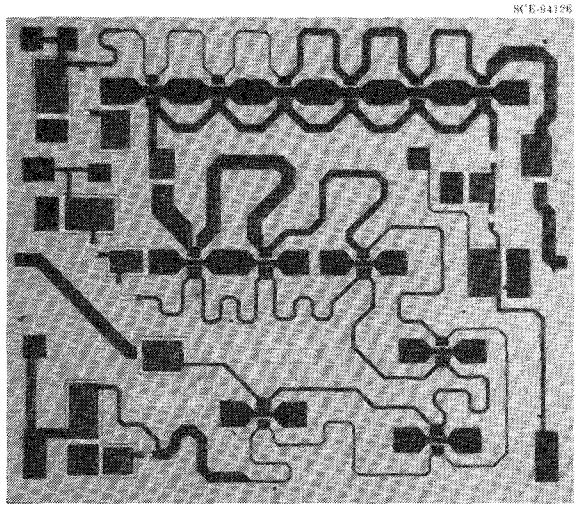

Figure 9. Photograph of 2-Stage Power Distributed Amplifier.

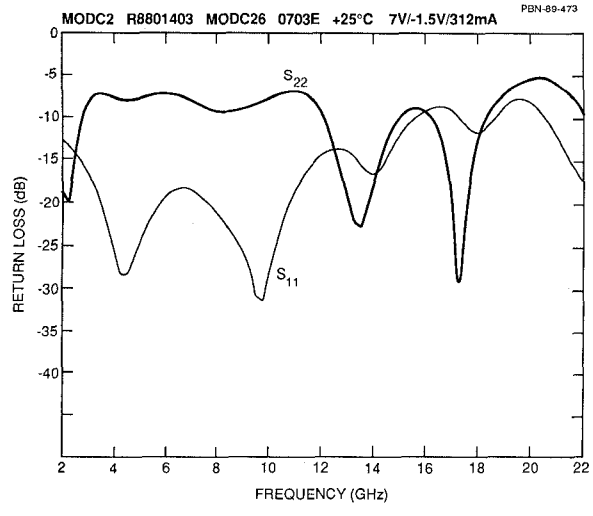

Figure 10. Measured Return Loss of Distributed Amplifier Designed for Power.

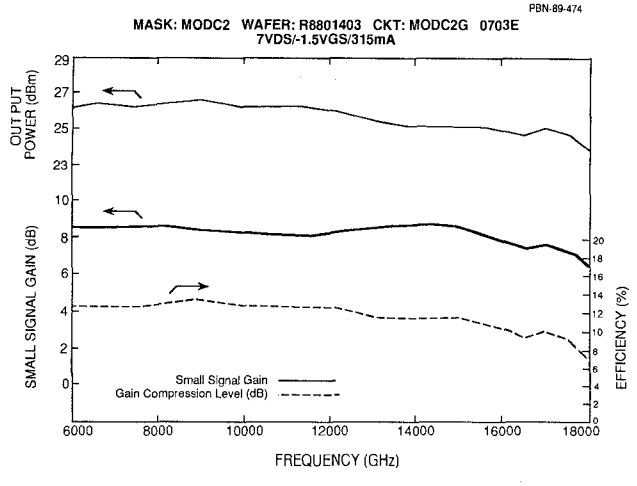

Figure 11. Measured Small Signal Gain, Output Power, and Efficiency of Distributed Amplifier Designed for Power Performance.